REMARKS

Applicant has reviewed the Office Action mailed on November 29, 2005 as well as the art cited. Claims 1, 43 and 49 have been amended, claim 8 has been cancelled. Claims 1-6, 9-32, 35-41, and 43-51 are pending in this application.

Rejections Under 35 U.S.C. § 103

Claims 1-6, 8, 28-32, 35-41, 43, 44, and 49-51 were rejected under 35 USC § 103(a) as being unpatentable over Ueda (U.S. Patent No. 5,787,118) in view of Coonce et al. (U.S. Patent No. 4,064,370). Applicant respectfully traverses this rejection.

Claim 1

Claim 1 has been amended to include a limitation of claim 8.

Regarding claim 1, the Examiner states that it would have been "obvious...to modify the equalizer of Ueda with the teachings of Coonce et al. in order to process each equalization data path in sequence (Coonce et al., Column 4, lines 62-64) and maintain synchronization between the data paths." Applicant respectfully traverses this assertion. Applicant respectfully asserts that Ueda does not need the buffers of Coonce et al. because Ueda does not need to "process each equalization data path in sequence."

Specifically, Ueda provides "an output selector switch [48] for selecting one of outputs produced from the equalized-output memory 43 and the equalized-output memory 44 in response to the output control signal supplied from the comparator 47." Col. 20, lines 28-31 (emphasis added). Thus, the Ueda does not need the buffers of Coonce et al. to process each equalization data path in sequence. Therefore, it would not have been obvious to modify Ueda with the buffers of Coonce et al. As a result, claim 1 should be allowed.

Claims 2-6 depend either directly or indirectly on claim 1 and, as a result, claims 2-6 should be allowed.

Claim 28

Regarding claim 28, the Examiner states that Ueda and Coonce et al. "disclose all the limitations of claims 28-32 (see rejections of claims 1, 6 and 8)." However, since there is no

motivation or suggestion to combine Ueda and Coonce et al., according to the argument presented for claim 1, and since neither Ueda nor Coonce et al. alone disclose all the limitations of claim 28, claim 28 should be allowed. Specifically, Ueda does not disclose "buffering the output of the plurality of equalizers, wherein buffering the output of the plurality of equalizers comprises buffering the output of the plurality of equalizers for the duration of a time slot of the communication channel."

Claims 29-32, 35 and 36 depend either directly or indirectly on claim 28 and, as a result, claims 29-32, 35 and 36 should be allowed.

Claim 37

Regarding claim 37, the Examiner states that Ueda and Coonce et al. "disclose all the limitations of claims 37-41 (see rejections of claims 1, 6 and 8)." However, since there is no motivation or suggestion to combine Ueda and Coonce et al., according to the argument presented for claim 1, and since neither Ueda nor Coonce et al. alone disclose all the limitations of claim 37, claim 37 should be allowed. Specifically, Ueda does not disclose "buffering the parallel outputs of the bank of adaptive equalizers... wherein buffering the parallel comprises buffering the parallel outputs for the duration of a time slot of the communication channel."

Claims 38-41 depend directly on claim 37 and, as a result, claims 38-41 should be allowed.

Claim 43

Claim 43 has been amended.

Regarding claim 43, the Examiner states that "the claimed apparatus includes features corresponding to the above rejections of claims 1 and 2." However, since there is no motivation or suggestion to combine Ueda and Coonce et al., according to the argument presented for claim 1, and since neither Ueda nor Coonce et al. alone disclose all the limitations of claim 43, claim 43 should be allowed. Specifically, Ueda does not disclose "buffering the parallel outputs of the bank of adaptive equalizers... wherein buffering the parallel comprises buffering the parallel outputs for the duration of a time slot of the communication channel."

Claim 44 depends directly on claim 43 and, as a result, claim 44 should be allowed.

Claim 49

Claim 49 has been amended.

Regarding claim 49, the Examiner states that "Ueda and Coonce et al. disclose all the limitations of claims 49-51 (see rejections of claims 1, 29, and 30)..." However, since there is no motivation or suggestion to combine Ueda and Coonce et al., according to the argument presented for claim 1, and since neither Ueda nor Coonce et al. alone disclose all the limitations of claim 49, claim 49 should be allowed. Specifically, Ueda does not disclose "a plurality of buffer circuits, each buffer circuit coupled between one of the plurality of equalizer circuits and the selector circuit to buffer the intermediate signals for a selected period of time."

Claims 50-51 depend directly on claim 49 and, as a result, claims 50-51 should be allowed.

Applicant may not have put forth responses to additional rejections to said claims at this time. However, the Applicant reserves the right to address said additional rejections to said claims if a further response is required.

Allowable Subject Matter

Application thanks the examiner for the indication that claims 9-27 and 45-48 are allowable.

CONCLUSION

Applicant respectfully submits that claims 1-6, 9-32, 35-41, 43-51 are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 332-4720.

Respectfully submitted,

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